GRINN
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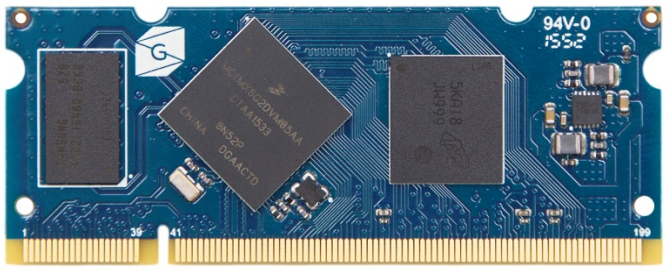
liteSOM

ARM Cortex-A7 System On Module

GLS SERIES DATASHEET



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1. Summary

1.1. Features

- Fast time to market
- Reduction of production costs
- Tiny size - 67.6mm x 26.5mm x 3mm
- SO-DIMM standard form factor
- Universal for multiple projects
- Fast and high-performance processor
- Easy EMC certification
- Low heat dissipation

1.2. Applications

- Industrial Automation
- Home/Building Automation
- Medical Appliances
- HMI panels
- Internet of Things
- Metering Gateways
- Consumer Electronics

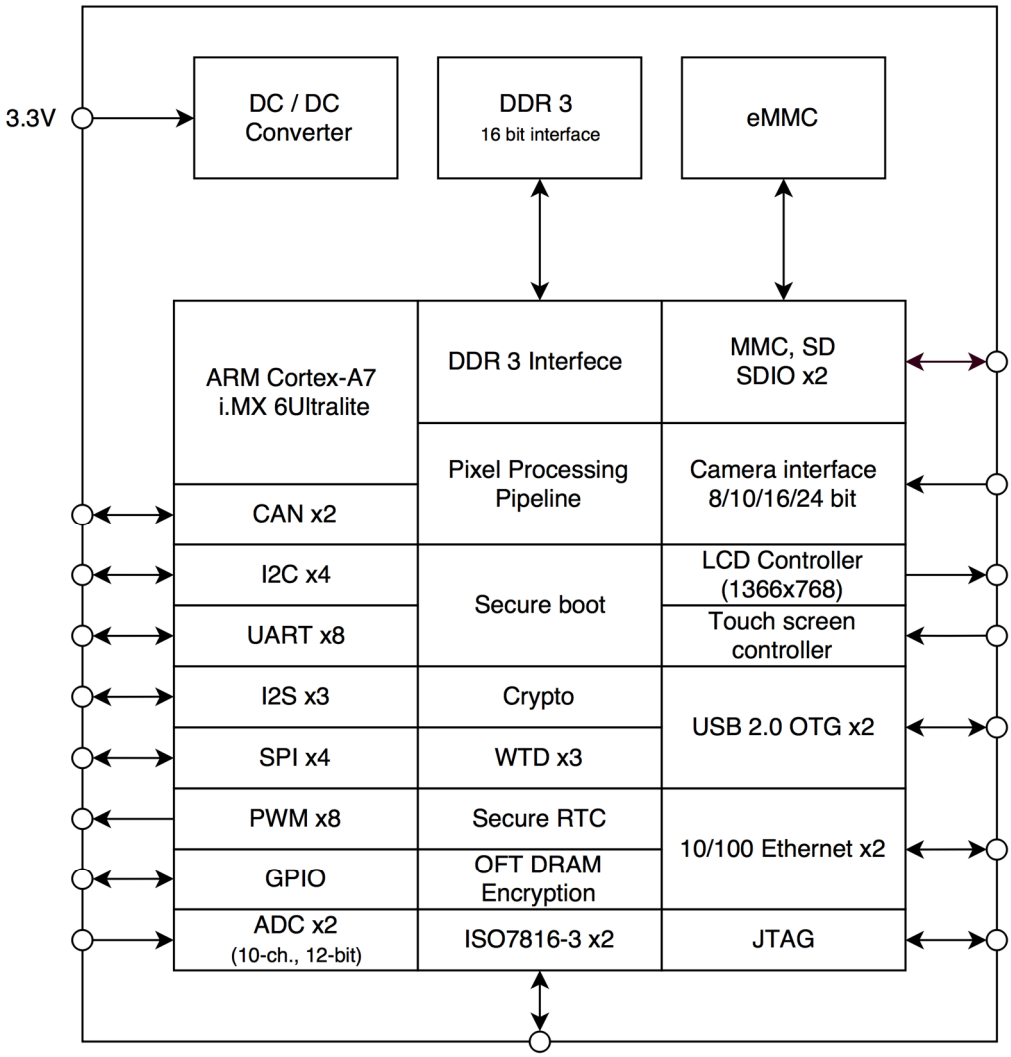
1.3. Description

The liteSOM is an extremely low-power, state-of-the-art module based on ARM Cortex-A7 core i.MX 6UltraLight processor. SO-DIMM form factor makes it easy to embed to your device without any technical issues. By placing the most critical signals in the module, even very complex peripherals can be placed using two PCB layers. This allows the delivery of cost-performance optimized designs and speeds-up time to market.
The liteSOM targets a wide range of industrial applications where price sensitivity of the product is important.
The module is designed to operate with all major OS. It is preconfigured for Linux. With a rich set of peripherals the module is designed to cater for a wide range of applications.

2. Functional Description

2.1. Block Diagram

The liteSOM functional block diagram is shown on figure below.



2.2. i.MX 6UltraLite Microprocessors

The liteSOM is based on NXP i.MX 6UltraLite microprocessor. It's powered by a high performance, ultra-efficient and low power ARM Cortex-A7 core which operates at speeds 528 MHz. The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Processor includes 16-bit LPDDR2, DDR3, DDR3L, raw and managed eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth™, GPS, displays and camera sensors.

2.3. RAM Memory

The liteSOM is available with up to 512MB of SDRAM DDR3 memory. The RAM memory is connected to i.MX 6UltraLite uses 16-bit interface running at frequency up to 400MHz, which gives bandwidth up to 12.8Gbit/s.

2.4. Flash Memory

The i.MX 6UltraLite supports external eMMC and NAND flash memory. The liteSOM is available with up to 2GB eMMC memory. The eMMC memory located on the liteSOM board enables direct system booting and user data storage.

3. Terminal Description

3.1. Pin out

Table below shows liteSOM pin assignments. For complete multifunction pins descriptions refer to section 4 in i.MX 6UltraLite Reference Manual.

Pin NO	Name	Type	i.MX 6UL ball	Description
1, 2, 19, 20, 27, 39, 41, 47, 48, 53, 54, 55, 58, 60, 61, 62, 64, 66, 67, 68 71, 72, 73, 75, 77, 78, 84, 86, 88, 90, 95, 96, 105, 111, 112, 114, 123, 124, 133, 134, 143, 144, 149, 151, 154, 156, 159, 160, 169, 172, 174, 179, 180, 185, 188, 190, 192, 194, 196, 198, 200	GND	Ground		Power ground
187, 189, 191, 1933, 195, 197, 199	3V3	Supply Input		+3.3V power supply input.
3	ONOFF	IO	R8	Power push-button input.
4	PORn	Input	P8	Reset.
5	BOOT_MODE1	IO	U10	Boot configuration.
6	SNVS_TAMPER7	Input	N10	Multifunction pin.
7	BOOT_MODE0	IO	T10	Boot configuration.
8	PMIC_STBY_REQ	Output	U9	Multifunction pin.
9	SNVS_TAMPER0	Input	R10	Multifunction pin.
10	PMIC_ON_REQ	Output	T9	Multifunction pin.
11	SNVS_TAMPER2	Input	P11	Multifunction pin.
12	SNVS_TAMPER1	Input	R9	Multifunction pin.
13	SNVS_TAMPER4	Input	P9	Multifunction pin.
14	SNVS_TAMPER5	Input	N8	Multifunction pin.
15	SNVS_TAMPER6	Input	N11	Multifunction pin.
16	SNVS_TAMPER3	Input	P10	Multifunction pin.

17	SNVS_TAMPER9	Input	R6	Multifunction pin.
18	SNVS_TAMPER8	Input	N9	Multifunction pin.
21	JTAG_TCK	Input	M14	JTAG test clock input.
22	JTAG_TMS	Input	P14	JTAG test mode select.
23	JTAG_TDI	Input	N16	JTAG test data input.
24	JTAG_TDO	Output	N15	JTAG test data output.
25	JTAG_TRSTn	Input	N14	JTAG test reset.
26	JTAG_MOD	Input	P15	JTAG mode
28	VCC_GPIO	Supply Input	J13	Supply GPIO port
29	GPIO9	IO	M15	Multifunction pin.
30	GPIO8	IO	N17	Multifunction pin.
31	GPIO7	IO	L16	Multifunction pin.
32	GPIO6	IO	K17	Multifunction pin.
33	GPIO5	IO	M17	Multifunction pin.
34	GPIO4	IO	M16	Multifunction pin.
35	GPIO3	IO	L17	Multifunction pin.
36	GPIO2	IO	L14	Multifunction pin.
37	GPIO1	IO	L15	Multifunction pin.
38	GPIO0	IO	K13	Multifunction pin.
40	VCC_UART	Supply Input	H13	Supply UART port
42	3V3_SNVS	Supply Input	P12	3V3_SNVS supply must be turned on before any other power supply
43	UART1_TX_DATA	IO	K14	Multifunction pin.
44	UART1_RTSn	IO	J14	Multifunction pin.
45	UART1_RX_DATA	IO	K16	Multifunction pin.
46	UART1_CTSn	IO	K15	Multifunction pin.
49	UART2_TX_DATA	IO	J17	Multifunction pin.
50	UART2_RTSn	IO	H14	Multifunction pin.
51	UART2_RX_DATA	IO	J16	Multifunction pin.
52	UART2_CTSn	IO	J15	Multifunction pin.

56	USB_OTG2_VBUS	Input	U12	USB2 OTG pin
57	USB_OTG2_D_P	IO	U13	USB2 data plus.
59	USB_OTG2_D_N	IO	T13	USB2 data minus.
63	USB_OTG1_D_P	IO	U15	USB1 data plus.
65	USB_OTG1_D_N	IO	T15	USB1 data minus.
69	nUSB_OTG1_CHD	Input	U16	USB1 charge detection.
70	USB_OTG1_VBUS	Input	T12	USB1 OTG pin
74	CCM_CLK1_N	IO	P16	Differential high speed clock Input/output[2]
76	CCM_CLK1_P	IO	P17	Differential high speed clock Input/output[2]
79	UART3_TX_DATA	IO	H17	Multifunction pin.
80	UART3_CTSn	IO	H15	Multifunction pin.
81	UART3_RX_DATA	IO	H16	Multifunction pin.
82	UART3_RTSn	IO	H15	Multifunction pin.
83	UART4_TX_DATA	IO	G17	Multifunction pin.
85	UART4_RX_DATA	IO	G16	Multifunction pin.
87	UART5_TX_DATA	IO	F17	Multifunction pin.
89	UART5_RX_DATA	IO	G13	Multifunction pin.
91	ENET1_TX_DATA1	IO	E14	Multifunction pin.
92	ENET1_TX_CLK	IO	F14	Multifunction pin.
93	ENET1_TX_DATA0	IO	E15	Multifunction pin.
94	ENET1_TX_EN	IO	F15	Multifunction pin.
97	ENET1_RX_DATA0	IO	F16	Multifunction pin.
98	ENET1_RX_ER	IO	D15	Multifunction pin.
99	ENET1_RX_DATA1	IO	E17	Multifunction pin.
100	ENET1_RX_EN	IO	E16	Multifunction pin.
101	ENET2_TX_CLK	IO	D17	Multifunction pin.
102	ENET2_TX_DATA0	IO	A15	Multifunction pin.
103	ENET2_TX_EN	IO	B15	Multifunction pin.
104	ENET2_TX_DATA1	IO	A16	Multifunction pin.
105	NVCC_ENET	Input	F13	Supply for Ethernet port

106	NAND_DQS	IO	E6	Multifunction pin[3].
107	ENET2_RX_ER	IO	D16	Multifunction pin.
108	ENET2_RX_DATA0	IO	C17	Multifunction pin.
109	ENET2_RX_EN	IO	B17	Multifunction pin.
110	ENET2_RX_DATA1	IO	C16	Multifunction pin.
113	NVCC_LCD	Input	E13	Supply LCD port
115	LCD_DATA23 BT_CFG4[7][1]	IO	B16	Multifunction pin and boot configuration.
116	LCD_DATA22 BT_CFG4[6][1]	IO	A14	Multifunction pin and boot configuration.
117	LCD_DATA21 BT_CFG4[5][1]	IO	B14	Multifunction pin and boot configuration.
118	LCD_DATA20 BT_CFG4[4][1]	IO	C14	Multifunction pin and boot configuration.
119	LCD_DATA19 BT_CFG4[3][1]	IO	D14	Multifunction pin and boot configuration.
120	LCD_DATA18 BT_CFG4[2][1]	IO	A13	Multifunction pin and boot configuration.
121	LCD_DATA17 BT_CFG4[1][1]	IO	B13	Multifunction pin and boot configuration.
122	LCD_DATA16 BT_CFG4[0][1]	IO	C13	Multifunction pin and boot configuration.
125	LCD_DATA15 BT_CFG2[7][1]	IO	D13	Multifunction pin and boot configuration.
126	LCD_DATA14 BT_CFG2[6][1]	IO	A12	Multifunction pin and boot configuration.
127	LCD_DATA13 BT_CFG2[5][1]	IO	B12	Multifunction pin and boot configuration.
128	LCD_DATA12 BT_CFG2[4][1]	IO	C12	Multifunction pin and boot configuration.
129	LCD_DATA11 BT_CFG2[3][1]	IO	D12	Multifunction pin and boot configuration.
130	LCD_DATA10 BT_CFG2[2][1]	IO	E12	Multifunction pin and boot configuration.
131	LCD_DATA9 BT_CFG2[1][1]	IO	A11	Multifunction pin and boot configuration.
132	LCD_DATA8 BT_CFG2[0][1]	IO	B11	Multifunction pin and boot configuration.
135	LCD_DATA7 BT_CFG1[7][1]	IO	D11	Multifunction pin and boot configuration.
136	LCD_DATA6 BT_CFG1[6][1]	IO	A10	Multifunction pin and boot configuration.
137	LCD_DATA5 BT_CFG1[5][1]	IO	B10	Multifunction pin and boot configuration.
138	LCD_DATA4 BT_CFG1[4][1]	IO	C10	Multifunction pin and boot configuration.
139	LCD_DATA3 BT_CFG1[3][1]	IO	D10	Multifunction pin and boot configuration.
140	LCD_DATA2 BT_CFG1[2][1]	IO	E10	Multifunction pin and boot configuration.
141	LCD_DATA1 BT_CFG1[1][1]	IO	A9	Multifunction pin and boot configuration.
142	LCD_DATA0 BT_CFG1[0][1]	IO	B9	Multifunction pin and boot configuration.

145	LCD_RESET	IO	E9	Multifunction pin.
146	LCD_VSYNC	IO	C9	Multifunction pin.
147	LCD_ENABLE	IO	D9	Multifunction pin.
148	LCD_HSYNC	IO	B8	Multifunction pin.
150	LCD_CLK	IO	A8	Multifunction pin.
152	NAND_WPn	IO	D5	Multifunction pin[3].
153	CSI_MCLK	IO	F5	Multifunction pin.
155	CSI_PIXCLK	IO	E5	Multifunction pin.
157	CSI_VSYNC	IO	F2	Multifunction pin.
158	CSI_HSYNC	IO	F3	Multifunction pin.
161	NVCC_CSI	Supply Input	F4	Supply Camera Sensor Interface
162	CSI_DATA0	IO	E4	Multifunction pin.
163	CSI_DATA2	IO	E2	Multifunction pin.
164	CSI_DATA1	IO	E3	Multifunction pin.
165	CSI_DATA4	IO	D4	Multifunction pin.
166	CSI_DATA3	IO	E1	Multifunction pin.
167	CSI_DATA6	IO	D2	Multifunction pin.
168	CSI_DATA5	IO	D3	Multifunction pin.
170	CSI_DATA7	IO	D1	Multifunction pin.
171	NVCC_SD	Input	C4	Supply external memory.
173	SD1_DATA0	IO	B3	Multifunction pin.
175	SD1_DATA2	IO	B1	Multifunction pin.
176	SD1_DATA1	IO	B2	Multifunction pin.
177	SD1_CMD	IO	C2	Multifunction pin.
178	SD1_DATA3	IO	A2	Multifunction pin.
181	SD1_CLK	IO	C1	Multifunction pin.
182	NAND_CLE	IO	A4	Multifunction pin[3].
183	NAND_CE0n	IO	C5	Multifunction pin[3].
184	NAND_CE1n	IO	B5	Multifunction pin[3].
186	NAND_REDYn	IO	A3	Multifunction pin[3].

(1) LCD_DATA[23:0] terminals are respectively BT_CFG1 [7:0] inputs, latched on power-up. External 10k-47k pull-up/pull-down resistors are needed on these terminals for proper boot configuration.
(2) Pins can be used to:
- feed external reference clock to the PLLs and further on to the modules inside SoC.
- output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals.

See the i.MX 6UltraLite Reference Manual (IMX6ULRM) for details on the respective clock trees.
(3) Pins belong to NVCC_NAND power group. This group is used to internal eMMC connection, which determinates power supply of 3.3V.

3.2. Boot Configuration Pins

Pins BOOT_MODE [1:0] are used to select system boot mode.

BOOT_MODE1	BOOT_MODE0	Boot Mode
LOW	LOW	Boot from Fuses
LOW	HIGH	Serial Downloader
HIGH	LOW	Internal Boot
HIGH	HIGH	Reserved

For complete Boot Mode configuration description see section 8 of i.MX 6UltraLite Reference Manual.

During the boot process on the first mode i.MX 6UltraLite processor senses BT_CFGx[7:0] configuration pins (see LCD_DATA[23:0] for pin description). It is latched on power-up state, thus every BT_CFGx[7:0] fuse should have external pull-up/pull-down resistor connected. For complete BT_CFGx[7:0] pin configuration description see section 5 of i.MX 6UltraLite Reference Manual.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

	min.	max.	unit
Supply voltage 3V3	-0.3	3.7	V
Supply Input Voltage to Secure Non-Volatile and Real Time Clock, 3V3_SNVS	-0.3	3.4	V
USB VBUS Supply, USB_OTGx_VBUS	-	5.35	V
IO Supply for GPIO Type Pins, NVCC _CSI, NVCC_LCD, NVCC_SD, NVCC_ENET, VCC_GPIO, VCC_UART	-0.5	3.7	V
Input/output Voltage range, V_{in}/V_{out}	-0.5	OVDD+0.3[1]	V
Current rating for liteSOM	-	870[2]	mA
Current rating for Secure Non-Volatile and Real Time Clock, 3V3_SNVS	-	500	mA
Current rating for USB_VBUS, USB_OTGx_VBUS	-	50[3]	mA
Current rating for GPIO Type Pins: NVCC _CSI, NVCC_LCD, NVCC_SD, VCC_GPIO, VCC_UART, NVCC_NAND, NVCC_ENET	-	Use maximum IO Eqation[4]	mA
Supply current ADC 3P3V	-	35	mA
Operating ambient temperature (commercial)	0	85	°C
Operating ambient temperature (extended)	-25	85	°C
Operating ambient temperature (industrial)	-40	105	°C

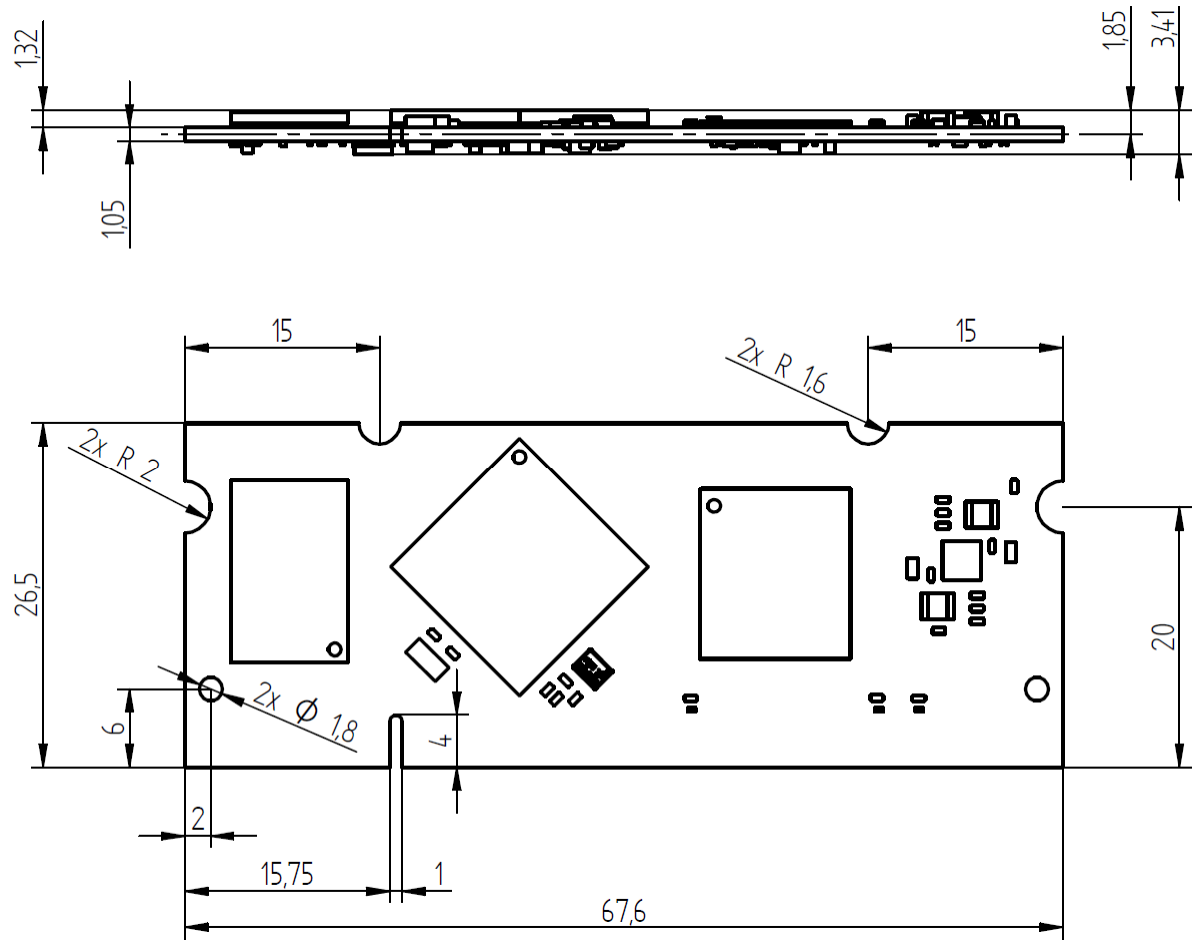
[1] OVDD is the I/O supply voltage.
[2] The maximum current may be higher depending on the specific operating configurations,
[3] This is the maximum current per active USB physical interface
[4] General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F) where:
N – Number of IO pins supplied by the power line
C – Equivalent external capacitive load
V – IO voltage
(0.5 x F) – Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz

4.2. Recommended Operating Conditions

	min.	nom.	max.	unit
Supply voltage, 3V3	3.0	3.3	3.6	V
Supply Input Voltage to Secure Non-Volatile and Real Time Clock, VDD_SNVS_IN, NVCC_NAND	3.0	3.3	3.4	V
USB VBUS Supply, USB_OTGx_VBUS	4.40	5.0	5.35	V
IO Supply for GPIO Type Pins, NVCC _CSI, NVCC_LCD, NVCC_SD, NVCC_ENET, VCC_GPIO, VCC_UART	1.65	1.8-3.3	3.6	V

5. Mechanical Characteristics

5.1. Technical drawing

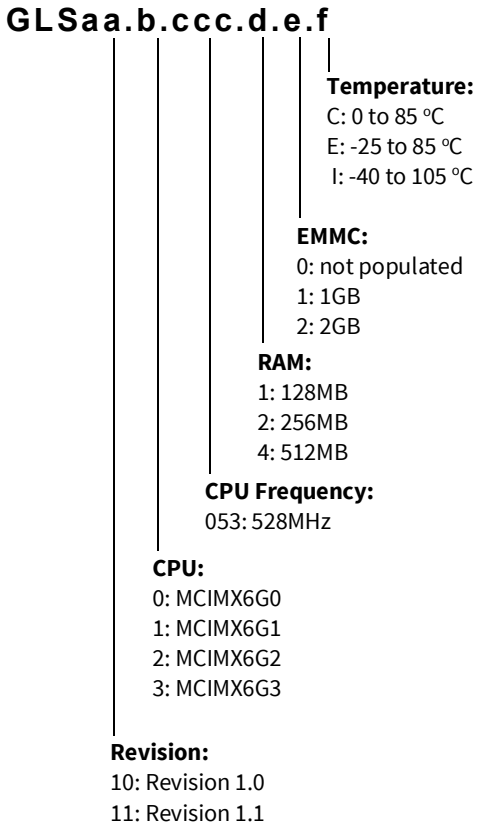


5.2. Sockets for the liteSOM

The liteSOM can be connected to board via the 200-pin SO-DIMM connector. This type of SO-DIMM connector is available in two variants DDR and DDR2. The liteSOM used standard DDR2. Grinn recommends using the TE Connectivity 1473005-4.

6. Ordering Information

6.1. Nomenclature



6.2. Order table

Order No	Processor	CPU Frequency	RAM	eMMC	Temperature
GLS11.2.053.2.2.E	MCIMX6G2CVM05AA	528 MHz	256 MB	2 GB	-25 to 85ºC
GLS11.2.053.2.0.I	MCIMX6G2CVM05AA	528 MHz	256 MB	-	-40 to 105ºC
GLS11.2.053.1.0.C*	MCIMX6G0CVM05AA	528 MHz	128 MB	-	0 to 85ºC

*minimum order quantity 1000 pcs

For other configurations please contact the distributor.

7. Reference Documentation

IMX6ULCAC i.MX 6UltraLite Applications Processors (Rev. 1)
IMX6ULRM i.MX 6UltraLite Reference Manual (Rev. 1)
IMX6ULCEC i.MX 6UltraLite Applications Processors for Consumer Products (Rev. 1 04/2016)

8. Document Revision History

Document Revision	Notes
1.0	Initial revision.

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